

DESCRIPTION

SMD-1G48は、512MビットDDR・DRAM（64M x 8bit）を16個搭載した128M x 64ビットDDR・DRAMモジュールです。

- ・ 184ピン・デュアル・インライン・メモリ・モジュール
(ピン・ピッチ 1.27mm)
- ・ 基板高 1.25" (31.75mm)
- ・ CL-tRCD-tRP=3-3-3 (PC3200)、2.5-3-3 (PC2700/PC2100)
- ・ 2.6V±0.1V単一電源 (PC3200)、2.5V±0.2V (PC2700/PC2100)
- ・ 8, 192リフレッシュ/64ms
- ・ SSTL_2コンパチブル
- ・ /CASレイテンシー3.0, 2.5, 2.0クロックプログラマブル (PC3200)
- ・ " 2.5, 2.0クロックプログラマブル (PC2700/PC2100)
- ・ 2バンク構成
- ・ アンバッファードタイプ
- ・ シリアルPD
- ・ 接続端子：電解金メッキ (t≥0.76μm)

Technical drawing of a PCB layout showing three views: FRONT, BACK, and SIDE.

FRONT View:

- Overall length: 133.35
- Overall width: 5.250
- Left side features a semi-circular cutout with a radius of 10.00 and a depth of 0.394.
- Right side features a semi-circular cutout with a radius of 10.00 and a depth of 0.394.
- Internal features include two rows of rectangular pads, each with a width of 2.50 and a spacing of 0.098.
- Dimensions for the right side cutout: 31.75, 1.250, 4.00, 0.157, 2.30, 0.91, 17.80, 0.700.

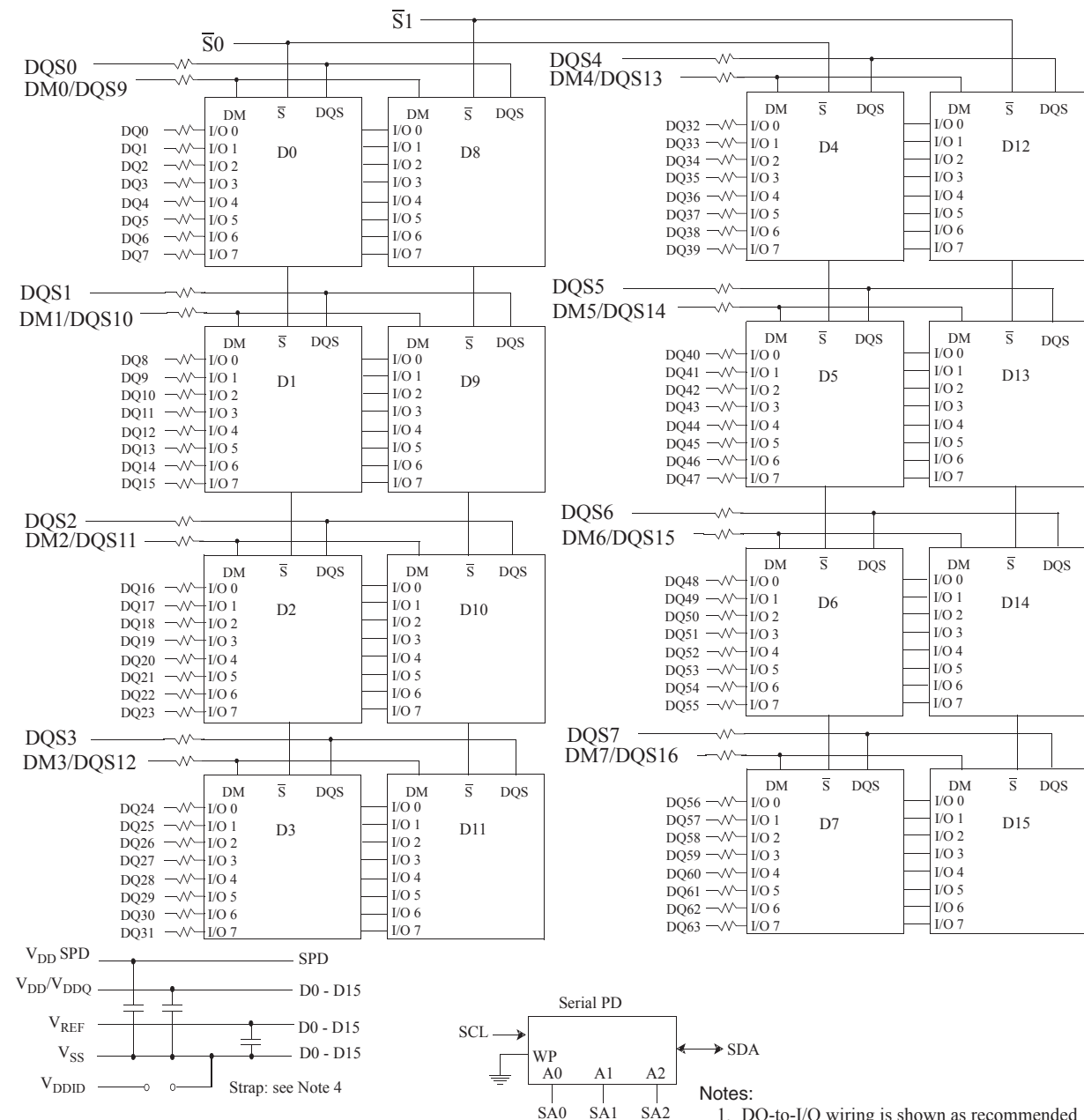
BACK View:

- Overall length: 133.35
- Overall width: 5.250
- Left side features a semi-circular cutout with a radius of 10.00 and a depth of 0.394.
- Right side features a semi-circular cutout with a radius of 10.00 and a depth of 0.394.
- Internal features include two rows of rectangular pads, each with a width of 2.50 and a spacing of 0.098.

SIDE View:

- Overall height: 4.00
- Overall width: 0.157 MAX
- Dimensions for the right side cutout: 1.27 +/- 0.10, 0.050 +/- 0.004.

Note: All dimensions are typical unless otherwise stated $\frac{\text{millimeters}}{\text{inches}}$

Functional Block Diagram

BA0 - BA1 → BA0-BA1: SDRAMs D0 - D15
 A0 - A12 → A0-A12: SDRAMs D0 - D15
 CEK1 → CEK: SDRAMs D8 - D15
 RAS → RAS: SDRAMs D0 - D15
 CAS → CAS: SDRAMs D0 - D15
 CEK0 → CEK: SDRAMs D0 - D7
 WE → WE: SDRAMs D0 - D15

* Clock Wiring	
Clock Input	SDRAMs
*CK0/CK0	4 SDRAMs
*CK1/CK1	6 SDRAMs
*CK2/CK2	6 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams

Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 ohms $\pm$ 5%.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
 STRAP OUT (OPEN): V_{DD} = V_{DDQ}
 STRAP IN (V_{SS}): V_{DD} $\neq$ V_{DDQ}
5. BA_x, A_x, RAS, CAS, WE resistors: 3 ohms $\pm$ 5%
 (Except PC2100)